Exhibit C

[redacted]

Exhibit B – Infringement of U.S. Patent No. 11,093,417

Netlist notes that these preliminary infringement contentions are based on publicly available information. Netlist expects that information to be revealed in future discovery may result in identification of additional instances of Micron's infringement, and may also enable identification of additional claims infringed by Micron. The claims asserted, and the theories set forth herein are based on Netlist's present understanding of the Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, these contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions. On information and belief, the examples are representative of the Accused LRDIMM products in material aspects.

The Accused Instrumentalities include Micron's Double Data Rate 4 ("DDR4") load reduced dual in-line memory modules ("LRDIMMs"). By way of non-limiting example, the accused DDR4 LRDIMM products include, without limitation, Micron products having the following part numbers: MTA36ASF4G72LZ-2G6, MTA36ASF4G72LZ-2G3, MTA72ASS8G72LZ-3G2, MTA72ASS8G72LZ-2G9, MTA72ASS8G72LZ-2G6, MTA72ASS8G72LZ-2G3, MTA36ASF8G72LZ-3G2, MTA36ASF8G72LZ-2G9, MTA144ASQ16G72LSZ-2S9, MTA144ASQ16G72LSZ-2S6, MTA72ASS16G72LZ-3G2, and MTA72ASS16G72LZ-2G9. The Accused Instrumentalities also include any other Micron DDR4 LRDIMM products made, sold, offered for sale, imported and/or used by Micron that are JEDEC-standard compliant memory modules. Examples of Micron's DDR4 LRDIMM products, reproduced below, can be found via Micron's module-selector web page. *See* Micron Website, https://www.micron.com/products/dram-modules.

Micron also infringes through acts of inducement and contributory infringement.

Claim 1	Evidence of Use
	See, e.g., JEDEC 82-32A Standard, p. 50 (annotated). The DDR4 data buffer is configured to add a predetermined amount of time delay **DWL** (DRAM Interface Write Leveling Control Word for each rank of the module ranks, *i.e.* Rank[3:0]) for each registered data transfer from the memory controller of the host system to a selected rank of memory devices through the circuitry in response to a write command, and to add a predetermined amount of time delay. **MRE** (DRAM Interface Receive Enable Control Word for each rank of Rank[3:0]) for each registered data transfer from a selected rank of memory integrated circuits to the memory controller of the host system through the circuitry in response to a read command. **DWL**: The DRAM Interface Write Leveling Training Mode determines an amount of time delay that is used to delay data strobes DQS signals used to register data signals DQ received from the computer system to be transferred to a selected rank of DDR4 SDRAM devices through the DDR4DB. Additional detailed descriptions are provided in section 2.20.2 of the JEDEC 82-32A Standard at pp. 30-31. **MRE**: The DRAM Interface MDQ Receive Enable Phase (MREP) Training Mode determines an amount of time delay that is used to delay DQS signals used to register DQ signals from the DDR4 SDRAM device to be sent to the computer system through the DDR4 DB. Additional detailed descriptions are provided in section 2.20.1 of JEDEC 82-32A Standard at pp. 29-30. Thus, the DDR4 data buffer is configured to add a predetermined amount of time delay **DWL** for each registered data transfer through the circuitry during write operations, and to add a predetermined amount of time delay **MRE** for each registered data transfer through the circuitry during read operations.